What is claimed is:

Sub A1

1. A method for processing instructions in a superscaler microprocessor, comprising:

selecting an initial sequence of instructions for inclusion in a trace cache line;

determining a set of rename resources needed for said trace cache line on a per-packet basis;

adding one or more provisional instructions to said trace cache line to create a provisional trace cache line;

repeating said determining step for said provisional trace cache line;

comparing said set of rename resources needed for said provisional trace cache line to a rename capacity; and

accepting said one or more provisional instructions for inclusion in said trace line and repeating said adding step, or rejecting said one or more provisional instructions, based on said comparing step.

2. A method in accordance with claim 1, wherein:

said set of rename resources needed and said rename capacity include a source parameter.

3. A method in accordance with claim 1, wherein:

said set of rename resources needed and said rename capacity include a destination parameter.

4. A method in accordance with claim 1, wherein:

said set of rename resources needed and said rename capacity include a line size parameter.

5. A method in accordance with claim 1, wherein:

determining a set of rename resources needed on a per-packet basis excludes destinations subsequently over-written within the packet from said set of rename resources needed.

6. A method in accordance with claim 1, wherein:

determining a set of rename resources needed on a per-packet basis excludes redundant sources within the packet from said set of rename resources needed.

7. A method in accordance with claim 1, wherein:

determining a set of rename resources needed on a per-packet basis excludes sources created within said trace cache line.

8. A method in accordance with claim 1, wherein:

selecting said initial sequence of instructions uses a worst case assumption of said set of rename resources needed.

9. A method in accordance with claim 1, wherein:

selecting said initial sequence of instructions includes tabulating a maximum rename resource cumulative total based on a plurality of instruction types.

10. A method in accordance with claim 1, wherein:

selecting a number of provisional instructions is performed based on a difference between said set of rename resources needed and said rename capacity.

11. An apparatus for processing instructions in a superscale microprocessor, comprising:

an instruction stream with a plurality of instructions;

a trace cache line for receiving said instructions from said instructions stream;

a packetized instruction resource calculator for determining a set of rename resources needed for said instructions in said trace cache line;

an instruction adder, responsive to said packetized instruction resource calculator, for adding one or more instructions to said trace cache line from said instruction stream while said set of rename resources needed is less than a rename resource capacity.

12. An apparatus in accordance with claim 11, wherein:

said set of rename resources needed includes a source parameter.

13. An apparatus in accordance with claim 11, wherein:

said set of rename resources needed included a destination parameter.

14. An apparatus in accordance with claim 11, wherein:

said set of rename resources needed includes a line size parameter.

15. An apparatus in accordance with claim 14, wherein:

said set of rename resources needed includes a source parameter.

16. An apparatus in accordance with claim 15, wherein:

said set of rename resources needed includes a destination parameter.

17. An apparatus in accordance with claim 11, wherein:

said packetized instruction resource calculator excludes destinations subsequently over-written within said trace cache line from said set of resources needed.

18. An apparatus in accordance with claim 17, wherein:

said packetized instruction resource calculator excludes redundant sources with said trace cache line from said set of resources needed.

19. An apparatus in accordance with claim 18, wherein:

said packetized instruction resource calculator excludes sources created within said trace cache line.

20. An apparatus in accordance with claim 11, further comprising:

a trace cache line initializer for initially loading said trace cache lien with an initial number of instructions.

21. An apparatus in accordance with claim 20, wherein:

said initial number of instructions is calculated as a fraction of said rename resource capacity.

22. A method of creating cache lines of instructions in a computer system, comprising:

determining the number of instructions in the cache lines using a packetization of instructions technique and a dynamic cache line size;

matching said dynamic cache line size to a rename unit capacity.

23. A method in accordance with claim 22, wherein:

matching said dynamic cache line size includes eliminating redundant register references within the cache lines.